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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/770,541	01/26/2001	Prithviraj Banerjee	NWU-P001	6788

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FERNANDEZ & ASSOCIATES LLP
1047 EL CAMINO REAL
SUITE 201
MENLO PARK, CA 94025

EXAMINER	
CHU, CHRIS C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 02/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/770,541	BANERJEE ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1 - 17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) 1 - 17 are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 January 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: On page 10, line 4 of the specification refers to a user-specification directives "36" which is not referenced in the figures. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description:

- In Fig. 2, the reference numbers "63" and "1" are not described in the specification of instant invention.
- In Fig. 11, the reference numbers "62," "64" and "66" are not described in the specification of instant invention.

A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Specification

4. The use of the trademark "MATLAB" has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Claim Objections

5. Claim 1 is objected to because of the following informalities: in claim 1, line 3, "andgenerating" should be --and generating--. Appropriate correction is required. Further, the phrase "such as" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1 ~ 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Panchul et al.

Regarding claim 1, Panchul et al. discloses in Fig. 2 and column 13, lines 29 ~ 63 computer-automated electronic design methodology comprising the steps of:

- accessing a first file (30) comprising an algorithm that is described in an array-oriented programming language such as MATLAB;
- and generating a second file (42) comprising a digital circuit representation that is synthesized automatically from the algorithm, where the representation is Register Transfer level VHDL or Verilog.

Regarding claim 2, Panchul et al. discloses in Fig. 2 and column 4, lines 51 ~ 67 the second file comprising a design feature for optimization that is described in an intermediate format.

Regarding claim 3, Panchul et al. discloses in Fig. 2 and column 13, lines 12 ~ 23 the second file being generated using a user directive (36), effectively allowing a user to guide a compiler by specifying a variable type or shape for optimization.

Regarding claim 4, Panchul et al. discloses in Fig. 2 and column 13, lines 29 ~ 43 in an electronic design system comprising a compiler for synthesizing a circuit definition from a high-level definition, a process comprising the step of: determining by a compiler (40) a type or a shape of a variable or an intermediate temporary variable.

Regarding claim 5, Panchul et al. discloses in Fig. 5A (at the for loop portion) electronic design scalarization process comprising the step of: transforming a first intermediate-format description into a second intermediate-format description by translating an array statement in the first intermediate-format description into a loop in the second intermediate-format description.

Regarding claim 6, Panchul et al. discloses in Fig. 5A in an automated design system comprising a processor for optimizing synthesis, a precision-inferencing method comprising the step of: determining by a processor a maximum bit precision for a variable for effecting a resource optimization.

Regarding claim 7, Panchul et al. discloses in Fig. 5A in an electronic design automation system comprising a compiler for processing a file including a real variable, an error-analysis method comprising the step of: determining a minimum number of bits for representing a real variable.

Regarding claim 8, Panchul et al. discloses in Fig. 5A compact electronic storage technique comprising the steps of:

- identifying a plurality of arrays having a bit precision that is less than an available memory width; and
- packing more than one array element into a memory location associated with the available memory.

Regarding claim 9, Panchul et al. discloses in Fig. 5A in an electronic design automation system, a levelization method comprising the step of; transforming a first statement in an intermediate-format description into a second statement associated with only one operation.

Regarding claim 10, Panchul et al. discloses in Fig. 5A in an electronic design automation system, a memory-access method comprising the step of: determining a memory access pattern or a memory access constraint for a design synthesis.

Regarding claim 11, Panchul et al. discloses in Fig. 5A in an electronic design automation system, a transformation method comprising the step of: transforming an intermediate format description for synthesizing an optimized memory access.

Regarding claim 12, Panchul et al. discloses in Fig. 5A in an electronic design automation system, a method comprising the step of; determining a number of states in a finite state machine realization associated with a transformed intermediate format description.

Regarding claim 13, Panchul et al. discloses in Fig. 5A in an electronic design automation system, a method comprising the step of: determining a finite state machine realization of one or more levelized statement in an intermediate format description.

Regarding claim 14, Panchul et al. discloses in Fig. 5A in an electronic design automation system, a method comprising the step of: determining a high-level variable or signal assignment for one or more variable in an intermediate format description.

Regarding claim 15, Panchul et al. discloses in Fig. 5A in an electronic design automation system, a method comprising the step of: identifying a pipeline opportunity in an intermediate format description.

Regarding claim 16, Panchul et al. discloses in Fig. 5A in an electronic design automation system, a method comprising the step of: transforming an intermediate format description to enable pipelining in a produced high-level code.

Regarding claim 17, Panchul et al. discloses in Fig. 5A in an electronic design automation system, a method comprising the step of: producing a pipelined high-level code from a transformed intermediate format description.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nagai, Richter et al. and Taylor disclose a hardware designs in high-level programming.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
January 28, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800